

Backend System Development for uGMRT

Harshavardhan Reddy, Sanjay Kudale, Nilesh Raskar, Shelton Gnanaraj, Navnath Shinde, Irappa Halagalli, Sandeep Chaudhari, Mekhala Muley, Sweta Gupta, Dnyandeo Nanaware, Kaushal Buch, Ajith Kumar, Yashwant Gupta Giant Metrewave Radio Telescope, NCRA-TIFR, Pune



Introduction: The Giant Metrewave Radio Telescope (GMRT) is a powerful Radio Telescope consisting of 30 parabolic dishes of 45 mtr diameter, spread over a region of 25 km diameter. The antennas are arranged in a Y shape with 12 antennas in a compact central array and 6 antennas in each arm of the "Y". The telescope currently operates at 5 different wave bands from 150 MHz to 1450 MHz with a maximum instantaneous bandwidth of 32 MHz. The signals from the antennas are down converted and processed using a Software based backend system (GSB) to generate interferometry and array outputs.

The GMRT is currently undergoing a major upgrade(uGMRT) to provide near seamless frequency coverage in the 50-1500MHz band and an instantaneous bandwidth of 400 MHz, with improved RFI rejection capabilities. The

upgraded receiver will provide many features like high dynamic range, improved channel resolution, reduced system complexity, highly flexible software based backends etc. The Backend Receiver system is a major component being upgraded as part of uGMRT and consists of analog processing section GAB (GMRT Analog Backend) and a digital processing section GWB (GMRT Wideband Backend).

The Backend system combines the signals from all antennas and gives out visibilities for each baseline which are recorded for offline processing. It allows multi-subarray mode of observation with independent control on each subarray. For spectral observations narrow band mode is supported. In the beam mode, signals from selected antennas are added to generate PA and IA beams.

Analog Backend System	Digital Backend System
Frequency conversion of RF signals received at Central Electronics Building (CEB) to Baseband.	Specifications: Number of stations : 32 Number of input polarizations : 2
Switchable attenuator to equalise the power given to ADC (takes care of receiver gain variations).	Number of input polarizations: 2CoarseCoarseCoarseCoarseDelayDe
Selectable filter bank to provide 100, 200, 400 MHz bandwidth signals to ADC.	Full Stokes capability : Yes Dump time : min 128 ms
LO frequency selection : option-1 common LO for all antennas	DelayFineFineFineFineCoarse and fine delay tracking: (+/-128 uS)DelayDelayDelayDelayFringe rotation: up to 5 HzandandandandWe have it himWe have it himWe have it himEtheEtheEtheEthe

option-2 individual for each antenna

Time & Frequency standard : option-1 GPS disciplined Rb oscillator option-2 Active Hydrogen Maser

Specifications:

Number of antennas	•	30
Number of Polarisations	•	2
ystem control	•	online
GPS/Rb based standard		
nput Frequency range	•	50 - 15
nput Power level	•	-24 dB
Output Frequency range	•	400 MI
Output Power level	•	-12 dBi
Output Bandwidth	•	100/200
witchable attenuation	•	+/ - 16dI
O common	•	10-150
O antenna specific	•	0.6 - 1.
vailable Headroom	•	27 dB



Power Monitoring: input & output

Noise+CW cal signal at GAB input

Noise cal signal at ADC input

System status monitoring

60-1 monitoring at GAB output

Implementation of Maser standard

independent for each channel

7 band pass filter selection

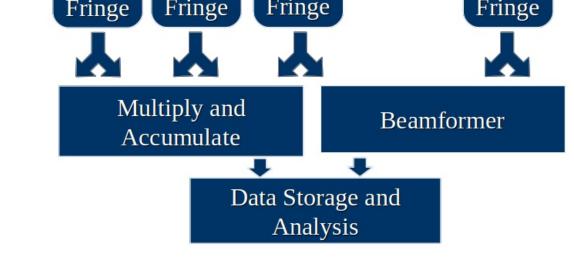
Fig1. 30 Antenna GAB system

Phase-2 Specifications:

LO selection

RF Filter bank

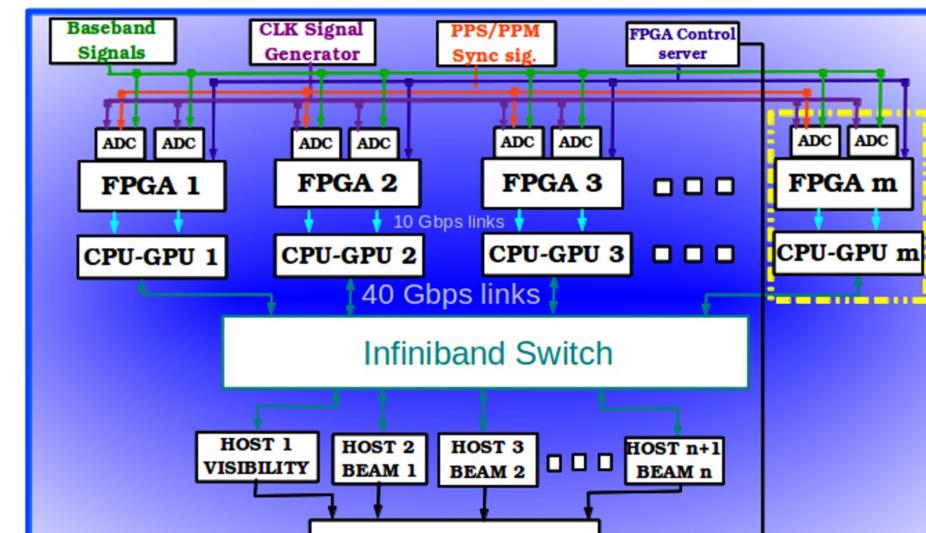
Walsh switching **RFI** Filtering Subarray support Narrowband modes





Design:

A hybrid design involving FPGAs and CPU-GPUs is used in GWB. FPGAs along with the ADCs perform the digitisation and packetising the data while CPU-GPUs perform correlation and record the visibilities onto a disk for post-processing and analysis. A scalable design is used in which FPGA and CPU-GPU boards can be added to take care of additional antennas when added to the system. The *figures* 6 and 7 depict the basic design and data flow in a single FPGA-CPU-GPU pair respectively. The design takes advantage of the high data rate interconnect of Infiniband and faster processing power of GPUs.

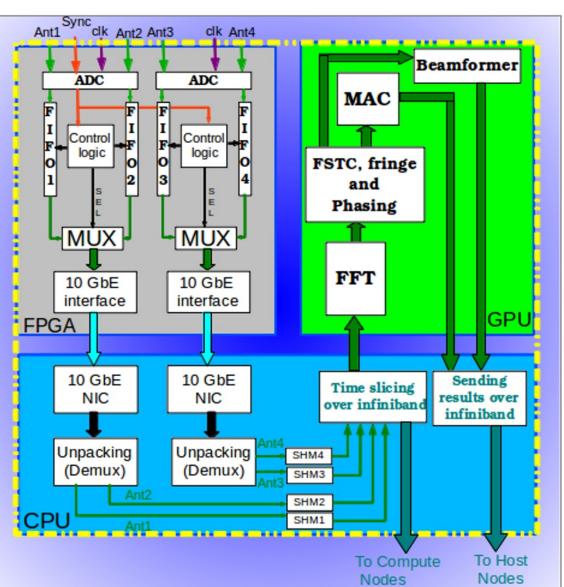


: Yes

: Yes

: Yes

: Yes



500 MHz 3m Hz m)0/400 MHz lB, 0.5dB step 00MHz, 1Hz step

- .5GHz,0.5MHz step

Var : +/-16dB SELECTABLE Step: 0.5dB **BB FILTER DIRECT PATH** TO DIGITAL BANK BACKEND SELECTABLE VARIABLE BW : 100, 200, 400 MHz (-12dBm) **RF FILTER** GAIN CONVERSION BANK STAGE BLOCK FROM **OF RECEIVER** (-24dBm@400MHz) SPARE OUTPUT (-12dBm) Phase – 1 MONITOR **NOISE IN** LO SIGNAL CIRCUIT

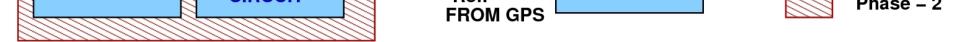


Fig2. Analog Backend block diagram

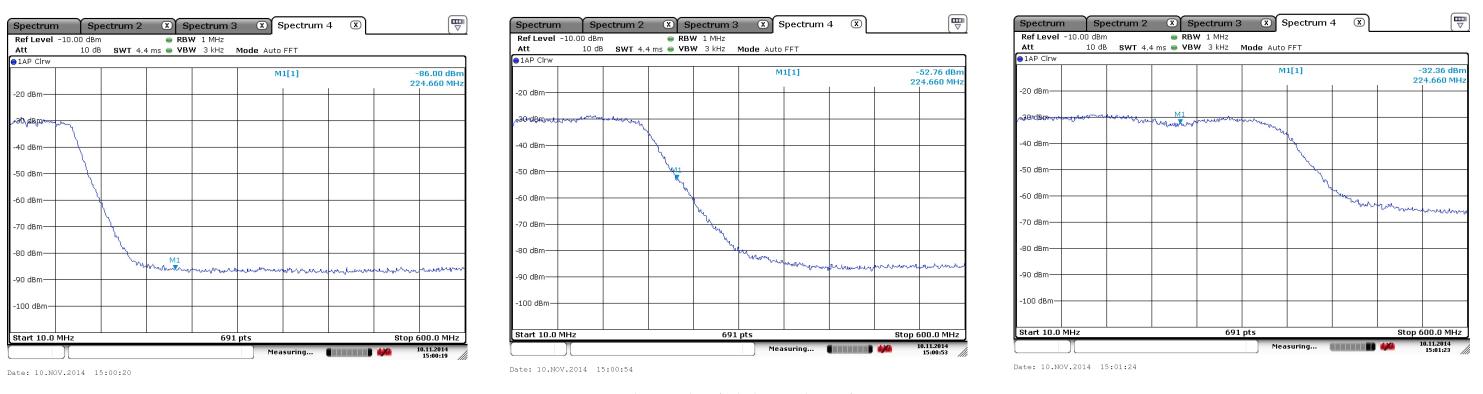
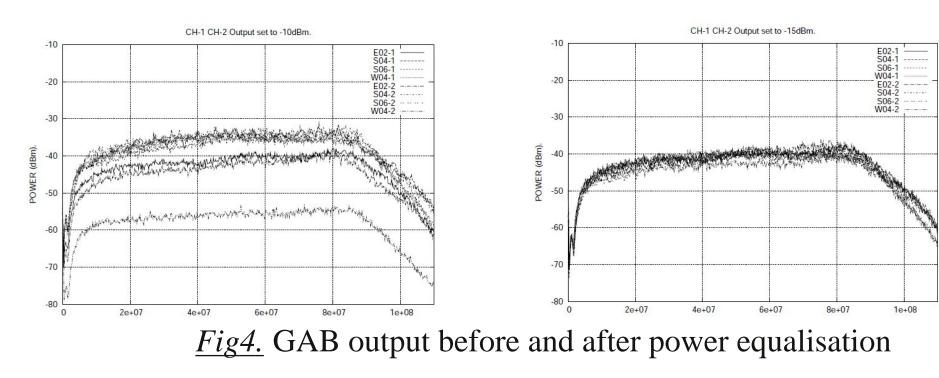


Fig3. GAB output bandwidth selection 100, 200, 400 MHz



Online server (Control Room) *Fig6*. GWB FPGA+GPU hybrid design for Digital Backend *<u>Fig7.</u>* Data flow in a single FPGA-CPU-GPU **Computation requirement at each stage :** No. of spectral channels, N No. of antennas, $N_a = 30$ = 32768No. of pols, $N_p = 2$ No. of beams, $N_{\rm h} = 1$ = 400 MHzBandwidth, v No. of stokes, N_s = 4 cops = complex operations per seconds FFT computation load $= 2vN_{a}N_{p}\log_{2}N cops$ = 3.1 Tflops MAC computation load $= vN_sN_a(N_a+1) cops = 6.6 T flops$ Fringe and FSTC correction = vN_aN_p cops = 102.4 Gflops = $vN_aN_p + vN_aN_p$ (multiply + add) cops Incoherent Beamformer = 153 Gflops = $vN_pN_bN_s + v(N_a + N_s)N_pN_b$ (multiply + add) cops Coherent Beamformer = 166 Gflops $= \sim 10$ Tflops **Total computation cost Data rate to be handled :** No. of CPU-GPUs, m = 16 No. of bits per sample, B = 4Sampling frequency, $F_s = 800 \text{MHz}$ Data rate between one FPGA board and a CPU-GPU, D_a = $N_a N_p F_s B$ bits/second = 12.8 Gbps $= D_a m$ bits/second Total data rate between FPGA boards and CPU-GPUs = 204.8 Gbps Bi-directional data rate between CPU-GPUs for time slicing and data sharing = $D_a(m-1)/m$ bits/second = 12 Gbps

Why GPUs :

GPU-accelerated computing is the use of a graphics processing unit (GPU) together with a CPU to accelerate scientific, analytics, engineering, consumer, and enterprise applications. It offers unprecedented application performance by offloading compute-intensive portions of the application to the GPU, while the remainder of the code still runs on the CPU. A CPU consists of a few cores optimized for sequential serial processing while a GPU has a massively parallel architecture consisting of thousands of smaller, more efficient cores designed for handling multiple tasks simultaneously.

Implementation :

A 16 ant, 2 pol, 200MHz bandwidth digital backend system has been implemented on Nvidia Tesla K20c GPUs hosted by eight Dell T620 servers with CASPER based Xilinx Virtex5 FPGA and ADC boards.

Results :

The backend system is used to process the GMRT antenna signals and the results are found to be as expected.



Fig8. CPU vs GPU



Fig9.16 antenna backend

A 32 ant, 2 pol, 400MHz bandwidth digital backend system is being developed with Walsh demodulation, RFI Filtering, Narrow band and multisubarray modes.

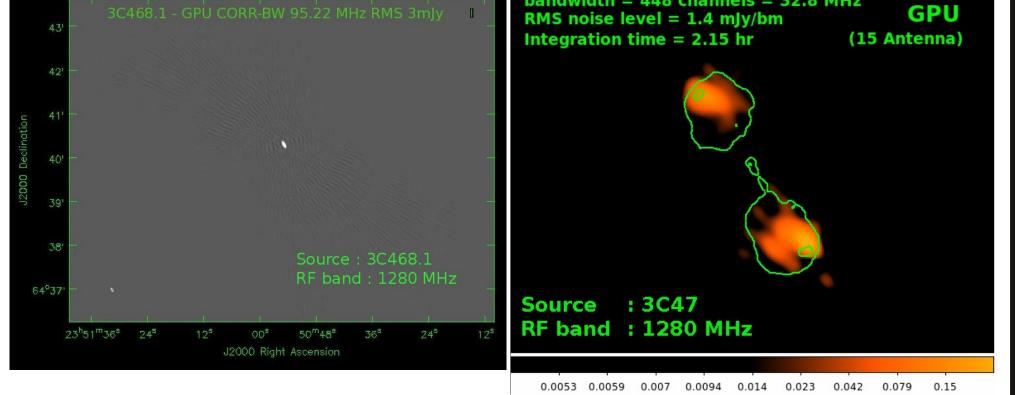
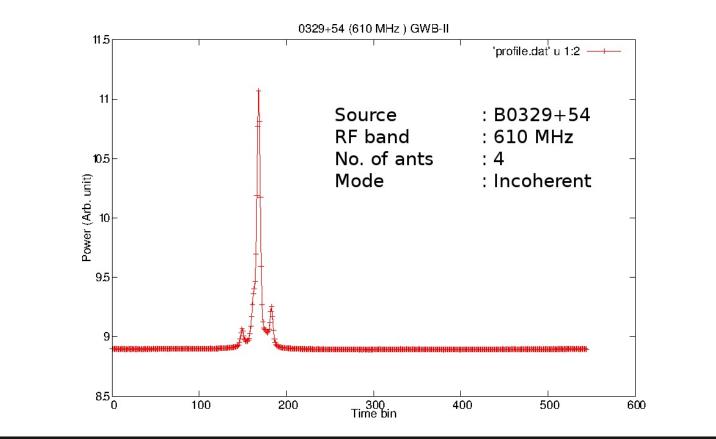


Fig10. Some early results

(Courtesy : Dharam Vir Lal)



Acknowledgements:

1. Swinburne University, Australia 3. CASPER Group 5. Mangesh Umbarje, GMRT, NCRA-TIFR 7. Jayanta Roy, NCRA-TIFR

2. Nvidia, India 4. Backend Group, GMRT 6. Sumit Mirajkar, GMRT, NCRA-TIFR 8. Dharam Vir Lal, NCRA-TIFR

References :

1. A real-time software backend for the GMRT, Jayanta Roy et.al 2010 2. http://www.nvidia.com/object/what-is-gpu-computing.html 3. https://casper.berkeley.edu/